SEMICONDUCTOR DEVICE WITH SPEED BINNING TEST CIRCUIT AND TEST METHOD THEREOF

Abstract of the Disclosure

A speed binning test circuit for a semiconductor device may include a plurality of circuit groups arranged along a boundary of a chip circuit. Each circuit group may include a different number of unit delay circuits that may form a chain structure. The speed binning test circuit may also include a plurality of pads. Each pad may be arranged between a pair of circuit groups so that at least one output terminal of a unit delay circuit of one of the plurality of circuit groups is connected to one of the pads. The speed binning test device performs a speed binning test method in which a signal through the circuit groups is delayed, and on-chip-variations are monitored to determine a total signal delay time through the chain structure.